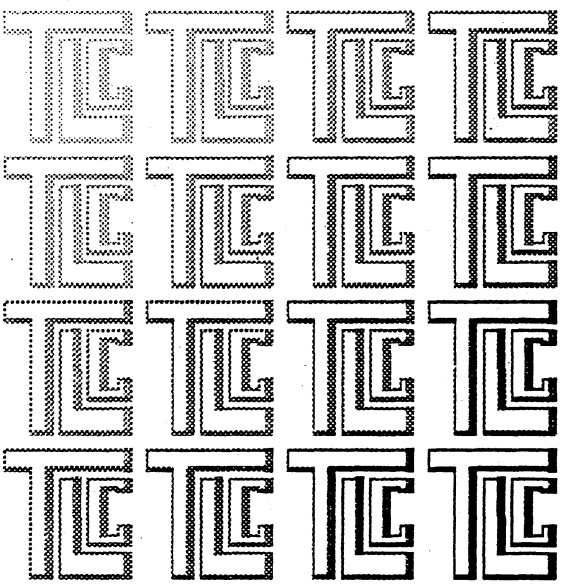
DCI-1300
DRV11/DR11-C for the PCI Local Bus
Owner's Manual



The **Logical** Company

DCI-1300-OM REV A

Owner's Manual for the
DCI-1300

DRV11/DR11-C Parallel Interface for the PCI Local Bus

The **Logical** Company

Document Number DCI-1300-OM
Revision A, March 1996

Service Information

If you cannot resolve problems with your unit, contact our Technical support department for assistance. Many times problems can be resolved with a single phone call. You can reach us at:

Telephone: +1 541-942-3610

Fax: +1 541-942-3640

Email: support@logical-co.com

Due to design complexity and the special equipment required to repair the unit, repairs must be made at our factory. If your product requires repair, call for an RMA number, and send it in the original packaging to the following address:

The Logical Company
75 Gateway Blvd.
Cottage Grove, OR 97424 USA

Please include the following information:

Your company name
Company address
Your name and telephone number
A brief description of the problem
The shipping address if different from above.

Our policy is to resolve problems as quickly and efficiently as possible.

Contents

Illustrations

Tables

1 Installation

This chapter lists the steps involved in installing the DCI-1300 hardware. Software driver installation is described in a separate publication. Refer to the appropriate manual for your system.

MED-0024-OM DCI-1300 OpenVMS Driver Manual
MED-0025-OM DCI-1300 OSF/1 AXP Driver Manual

References throughout this chapter tell you where to look for more detailed information. The DCI-1300 module is shown in Figure 1-1. Refer to this figure as you follow the steps outlined below.

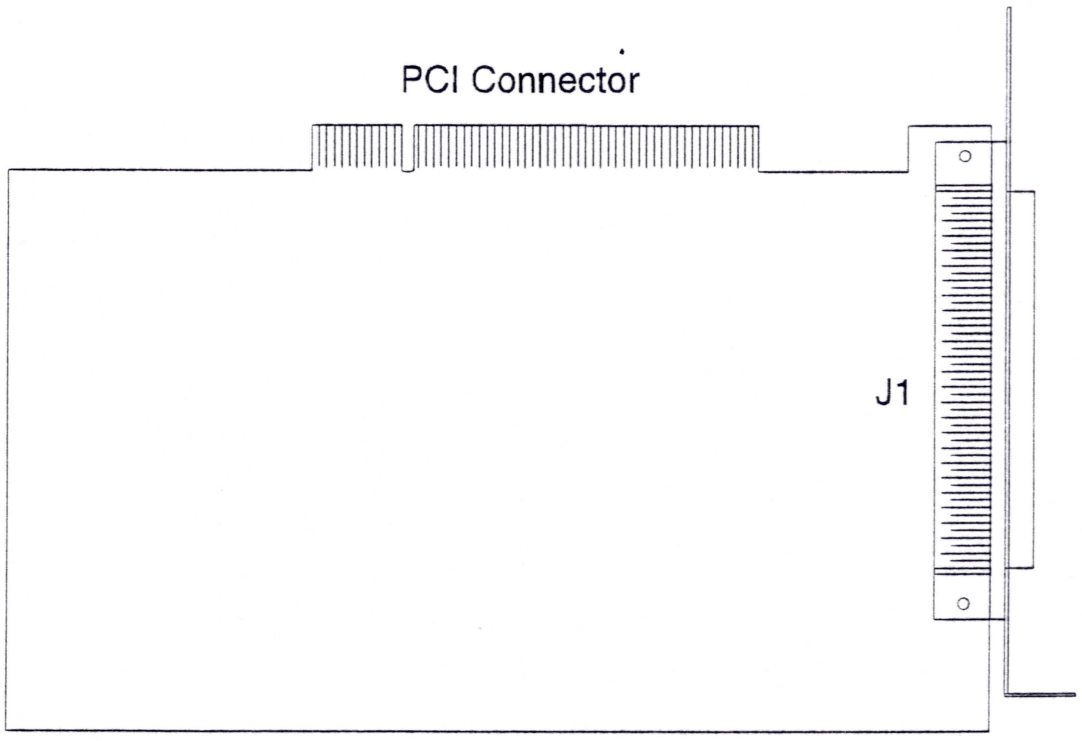


Figure 1-1: DCI-1300 Module

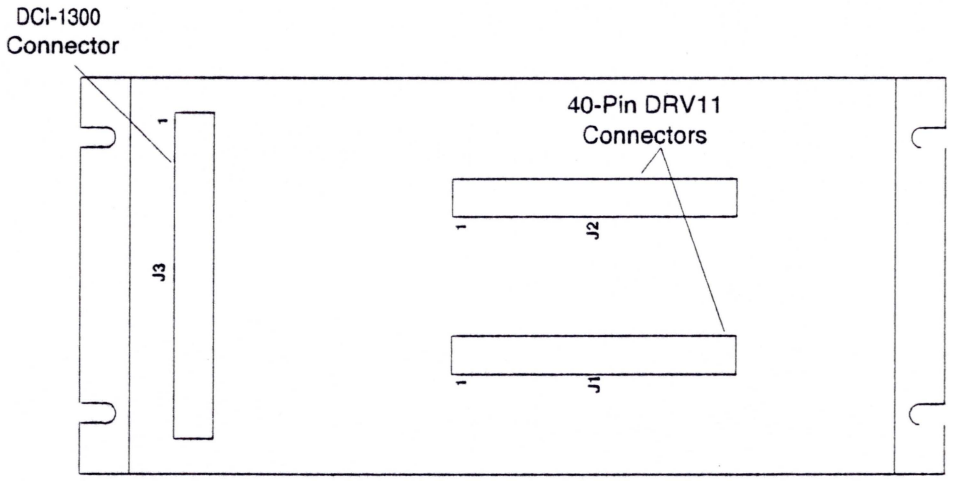


Figure 1-2: CPX-1303 Adapter Panel

1. Open the workstation enclosure or expansion chassis

To remove the cover from the workstation or expansion chassis enclosure:

A. Shut down the system software as described in the instructions that came with your software.

B. Remove power to the system unit or expansion chassis.

C. Open the enclosure as described in the manual that came with the unit.

Note: Use the anti-static wrist strap supplied with your system unit to prevent damage to the equipment. Clip the free end of the strap to the metal frame of the enclosure.

2. Install the DCI-1300 module.

The DCI-1300 may be installed in any available PCI Local Bus option slot.

A. If the back of the expansion chassis or system unit has a metal cover plate over the opening of the PCI slot you have selected, remove the anchor screw that holds the cover in place then slide the cover out of the slot.

B. Position the DCI-1300 with the gold fingers on the edge of the module next to the PCI connector of the selected slot . Gently rock the module into the PCI connector while you fit the metal bulkhead into the slot opening. Be sure that the connectors are firmly seated.

Note: If the enclosure contains RFI clips along the slot, take care when inserting the module not to push the clips out of alignment.

C. Secure the DCI-1300 using the anchor screw that you removed in Step A. Retain the cover plate for future use.

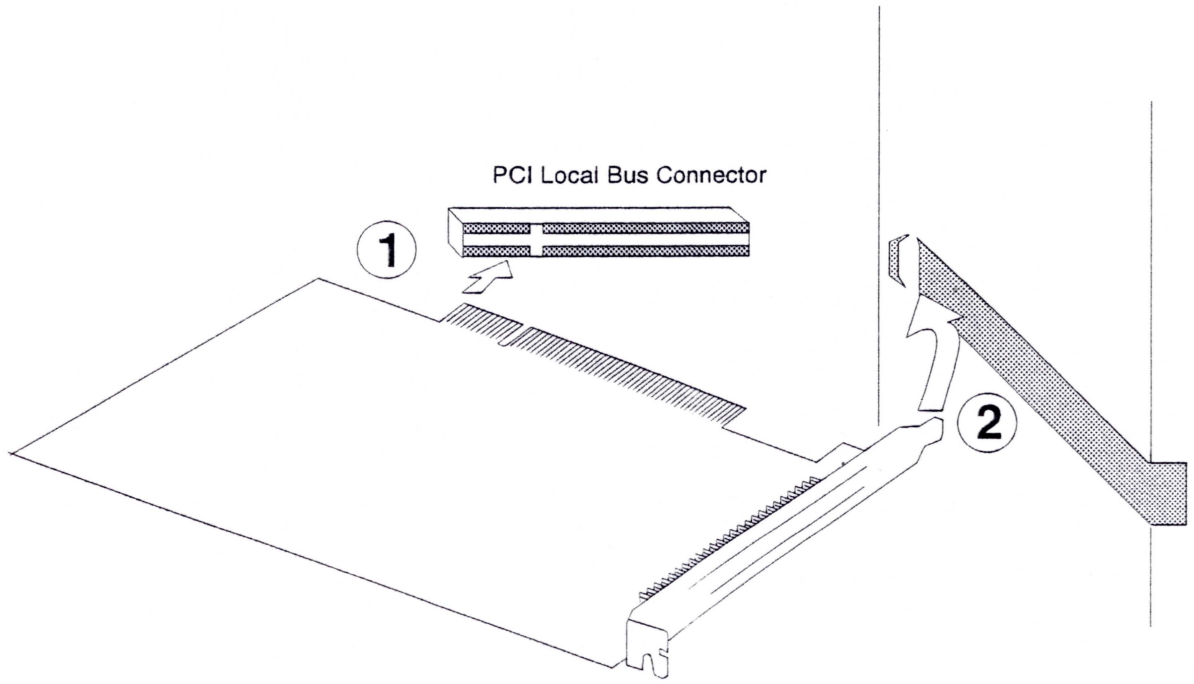


Figure 1-3: Inserting the Board into the PCI Slot

D. Remove the anti-static wrist strap, replace the cover on the enclosure and secure.

You are now ready to connect the data cables.

3. Cable controller to the adapter panel

Use the supplied 8-foot cable to connect the workstation to the CPX-1303 adapter panel. The adapter panel is provided with screw slots for RETMA rack mount or wall mount. It also has no-mar feet for desktop or floor use.

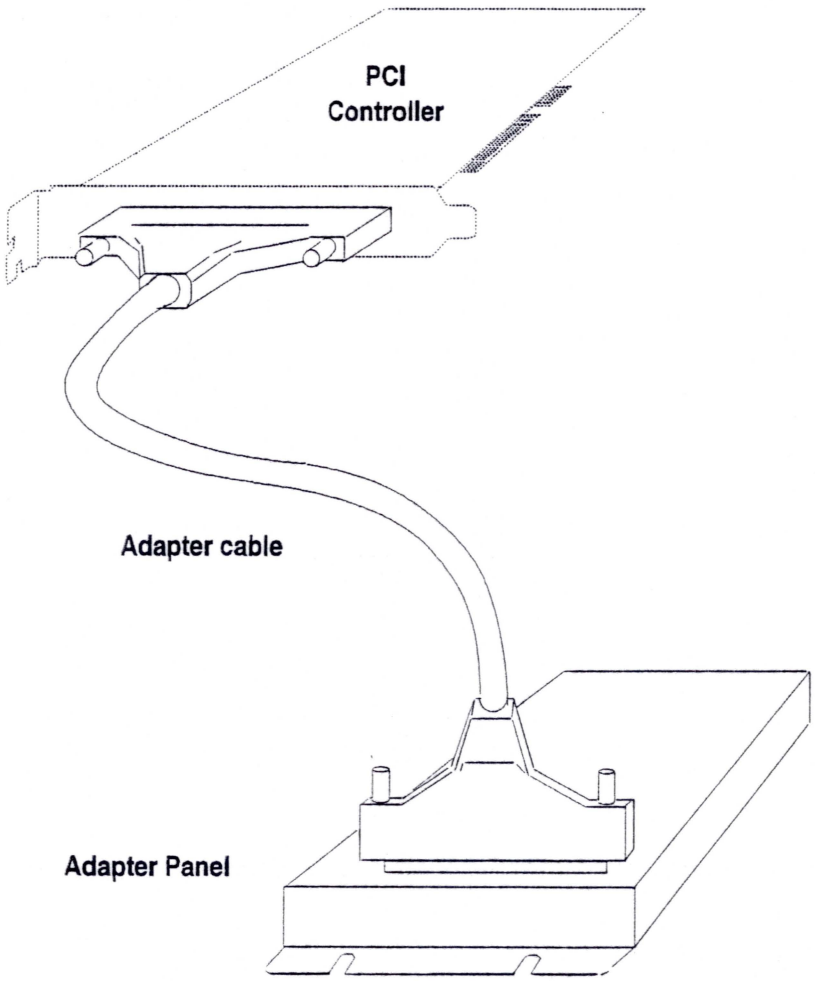


Figure 1-4: Cabling the Adapter Panel

4. Cable the CPX-1303 adapter to user equipment

Use two 40-pin cables to connect the user equipment to the DCI-1300 adapter panel. The function of each interface signal is described in Chapter 2.

J1 and J2 on the CPX-1303 adapter panel correspond to J1 and J2 on Digital's DRV11, DR11-C. Connect user cables to the adapter the same as you would connect to a DRV11 or DR11-C. If you are unsure, refer to the connector pin assignments in Appendix B.

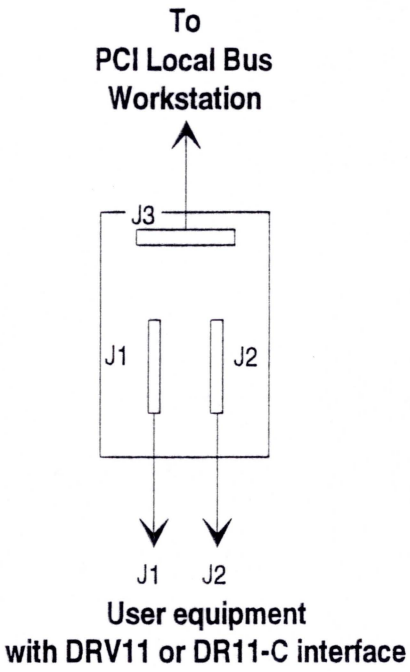


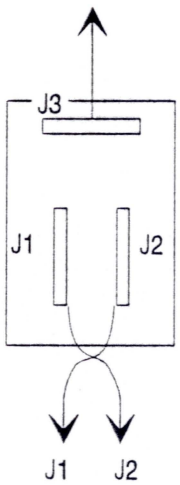
Figure 1-5: Cabling the CPX-1303 Adapter Panel to User Equipment

5. Cable the CPX-1303 adapter to a remote computer.

Use two 40-pin cables to connect the remote system to the DCI-1300 adapter panel. The function of each interface signal is described in Chapter 2.

J1 and J2 on the CPX-1303 adapter panel correspond to J1 and J2 on Digital's DRV11 or DR11-C. Connect user cables to the adapter crossing the cables as shown in Figure 1-7. If you are unsure, refer to the connector pin assignments in Appendix B.

Note that when the cables are crossed, the triangles do not align at one end of each cable. Pin 1 mates with pin 40.



Remote workstation or computer system with DRV11 or DR11-C interface

Figure 1-6: Cabling the CPX-1303 to a Remote System

6. Power up the system and verify installation.

The following conventions are used in this manual:

`output`	In examples, computer output is shown in this type.
`user input`	In examples, user input is shown in bold type.
`[CR]`	This is used to specify pressing the Return/Enter key.

A. Apply power to the computer system and wait for the self-test to complete.

B. To verify that the DCI-1300 is recognized by the system and to confirm the physical slot number, use the console show config command.

```
P00>>>show config
                        Digital Equipment Corporation
                            AlphaServer 2000 4/200

SRM Console V3.9-89                VMS PALcode X5.48-89, OSF PALcode X1.35-55

Component    Status              Module ID
CPU 0          P                 B2020-AA DECchip (tm) 21064-3
Memory 0       P                 B2023-BA  64 MB
I/O                              B2111-AA
                                 dva0.0.0.0.1              RX26

 Slot  Option                    Hose 0, Bus 0, PCI
   1   NCR 53C810                pka0.7.0.1.0              SCSI Bus ID 7
                                 dka0.0.0.1.0              RZ28
                                 dka600.6.0.1.0            RRD43
                                 mka500.5.0.1.0            TLZ06
   2   Intel 82375EB                                       Bridge to Hose 1, EISA
   6   DECchip 21040-AA          ewa0.0.0.6.0              08-00-2B-E4-23-F9
   8   000710E8

 Slot  Option                    Hose 1, Bus 0, EISA
   7   CPQ3011
```

The console firmware found a DCI-1300 (option 000710e8) in PCI slot 8. The AlphaServer 2000 labels PCI backplane slots 6-8 as module bulkheads PCI0-PCI2 on the rear of the chassis. Please note that the internal backplane slot number is used for all hardware and software installation. For other PCI based Alpha systems, refer to the owner's guide delivered with the system for the PCI slot numbering convention.

C. The DCI-1300 is supplied with a loopback cable to allow you to run the loopback diagnostics supplied with all DCI-1300 device drivers. Refer to the owner's manual supplied with the driver for information on the installation and operation of the diagnostic.

2 General Description

The DCI-1300 is a general purpose interface for transferring data directly between the PCI Local Bus and a user's device.

The DCI-1300 is signal and pin compatible with Digital's DRV11 and DR11-C controllers to facilitate the migration of user equipment from existing Unibus and Q-bus systems to the newer workstations such as the Alpha supporting the PCI Local Bus.

The DCI-1300 is contained on a standard short PCI card. The controller contains a 100-pin, high density connector for external connection to user input and output signals. An 8-foot cable connects the DCI-1300 controller to an external adapter panel. The adapter panel provides two DRV11 and DR11-C compatible 40-pin flat ribbon connectors used to connect to user equipment.

The DCI-1300 controller contains four internal registers that provide the necessary controls and status to perform data transfers to or from the PCI Local Bus and to transfer 16-bit data between the DCI-1300 and external user equipment. The four internal registers are a control and status register (CSR), a data output register (DOUT), a data input register (DIN), and a timer register (TMR).

User Interface Signals

Table 2-1 lists the interface signals used by the DRV11 and DR11-C. DR11-C signals are shown in parenthesis when different from DRV11.

Mnemonic	Description
OUT00-H - OUT15-H	Output data lines to user device. High true, one = high. These lines transmit the current contents of the DOUT register to the user device.
IN00-H - IN15-H	Input data lines from the user device. High true, one = high. These lines transmit information from the user device when host software reads the DIN register.
NEWDARDY-H (NEWDATARDY-H)	Output signal to the user device. High true. This pulse is sent to inform the user device that new data has been written into the output data register and is available on the output data lines. The DCI-1300 may change the data after the trailing edge of the signal. The duration of this pulse is controlled by the TMR register.
DATRANS-H (DATA TRANS-H)	Output signal to the user device. High true. This pulse is sent to inform the user device that the input data buffer is being read and the DCI-1300 is ready to accept data on the input data lines. The user device can change the data after the trailing edge of the signal. The duration of this pulse is controlled by the TMR register.
CSR1-H	Output signal to the user device. High true, one = high. This signal is controlled by the host software by writing into bit 01 of the CSR and the function is user defined.
CSR0-H	Output signal to the user device. High true, one = high. This signal is controlled by the host software by writing into bit 00 of the CSR and the function is user defined.
INIT-H (AINIT-H)	Output signal to the user device. High true. Set when the PCI reset signal is set.
INITV2-H (BINIT-H)	Output signal to the user device. High true. Set when the PCI reset signal is set.
REQA-H	Input signal from the user device. High true. This signal is controlled by the user device and is host software readable as bit 07 of the CSR. When asserted, a PCI interrupt request is generated if IEA (CSR bit 06) is set.
REQB-H	Input signal from the user device. High true. This signal is controlled by the user device and is host software readable as bit 15 of the CSR. When asserted, a PCI interrupt request is generated if IEB (CSR bit 05) is set.

Table 2-1: User Interface Signals

Specifications

Physical

Dimensions	Standard PCI short card measuring 6.875 inches by 4.2 inches (17.46 cm by 10.67 cm).

Interface

DCI-1300-A Controller	100-pin high density connector
CPX-1303 Panel	Provides user connection to two 40-pin DRV11 and DR11-C style connectors.
Cable (CAB-1104-8)	8-foot terminated with 100-pin connector at both ends.

Electrical

Power Required:	
+5 volts DC	2 amps

Performance

Throughput	Up to 200K 16-bit words per second (operating system overhead will reduce performance)

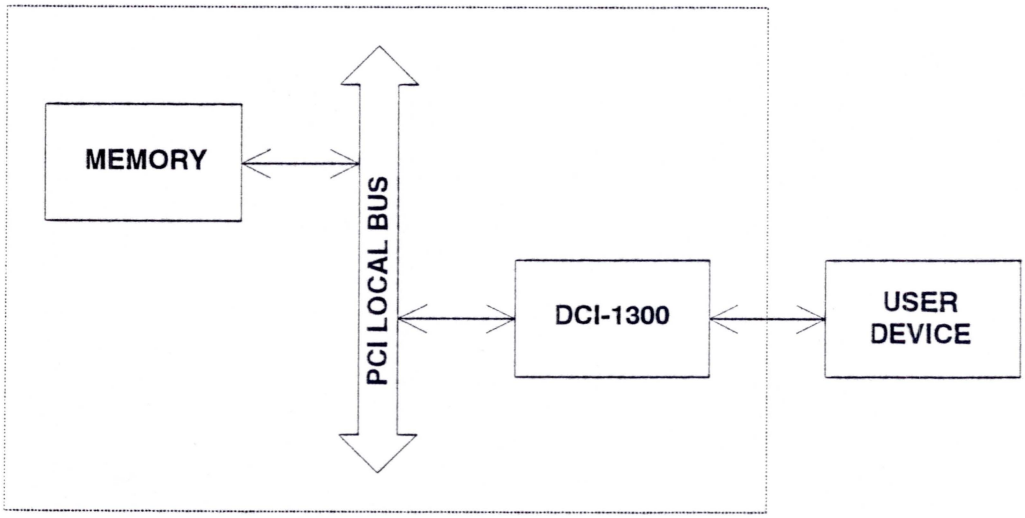
Environmental

Operating Conditions:	
Temperature	5° to 50° C (41° to 122° F)
Relative Humidity	20% to 80% noncondensing
Storage Conditions:	
Temperature	-40° to 66° C (-40° to 150° F)
Relative Humidity	10% to 95% noncondensing

3 Application

The DCI-1300 can be used to connect user's equipment to the PCI Local Bus for high speed parallel data transfers. The DCI-1300 is capable of transferring 16-bit data to or from the user's equipment. The DCI-1300 is signal and pin compatible with Digital's DRV11 and DR11-C interfaces and can operate with most user equipment that is designed to operate with Digital's DR11-C and DRV11. This provides a migration path from the Unibus or Q-bus systems to the PCI Local Bus. Data can be transferred between the user device and the PCI Local Bus at rates up to 200K words/sec, however, operating system overhead will reduce the performance. Refer to the applicable device driver manual for specific throughput. The DCI-1300 is connected to the user device using two 40-pin flat ribbon cables up to 25 feet in length.

The DCI-1300 is also capable of being used as an interprocessor link (non-DECnet) between two systems by cabling a DCI-1300 to another DCI-1300, a DRV11, or a DR11-C. The OpenVMS operating system does not provide software support for interprocessor links. You must write the code for any interprocessor communications operations. Figures 3-1 and 3-2 show two typical applications of the DCI-1300.



Data Interface

Figure 3-1: Typical Data Interface Application

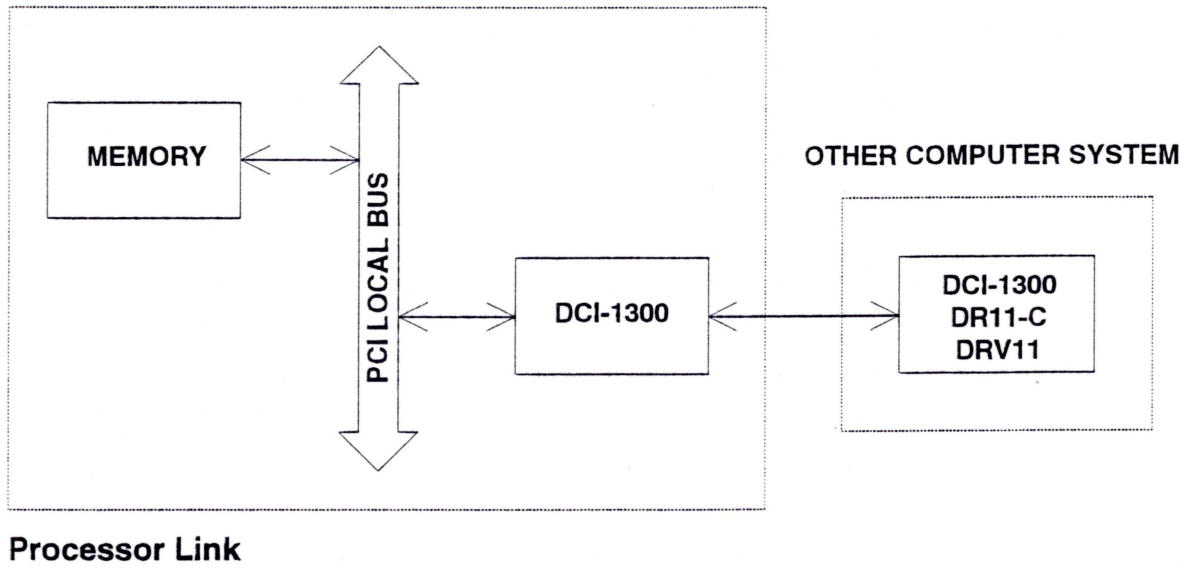


Figure 3-2: Typical Processor Link Application

4 Registers

Register Description Format

The DCI-1300 contains three major groups of registers: PCI configuration registers, PCI operation registers, and device registers. The following pages describe the operation of each group of registers.

PCI Bus Configuration Registers

The DCI-1300 controller contains a unique 256-byte region called configuration header space. Portions of this configuration header space are mandatory in order for a PCI controller to be in full compliance with the PCI specification. This section describes each register contained within the configuration register set.

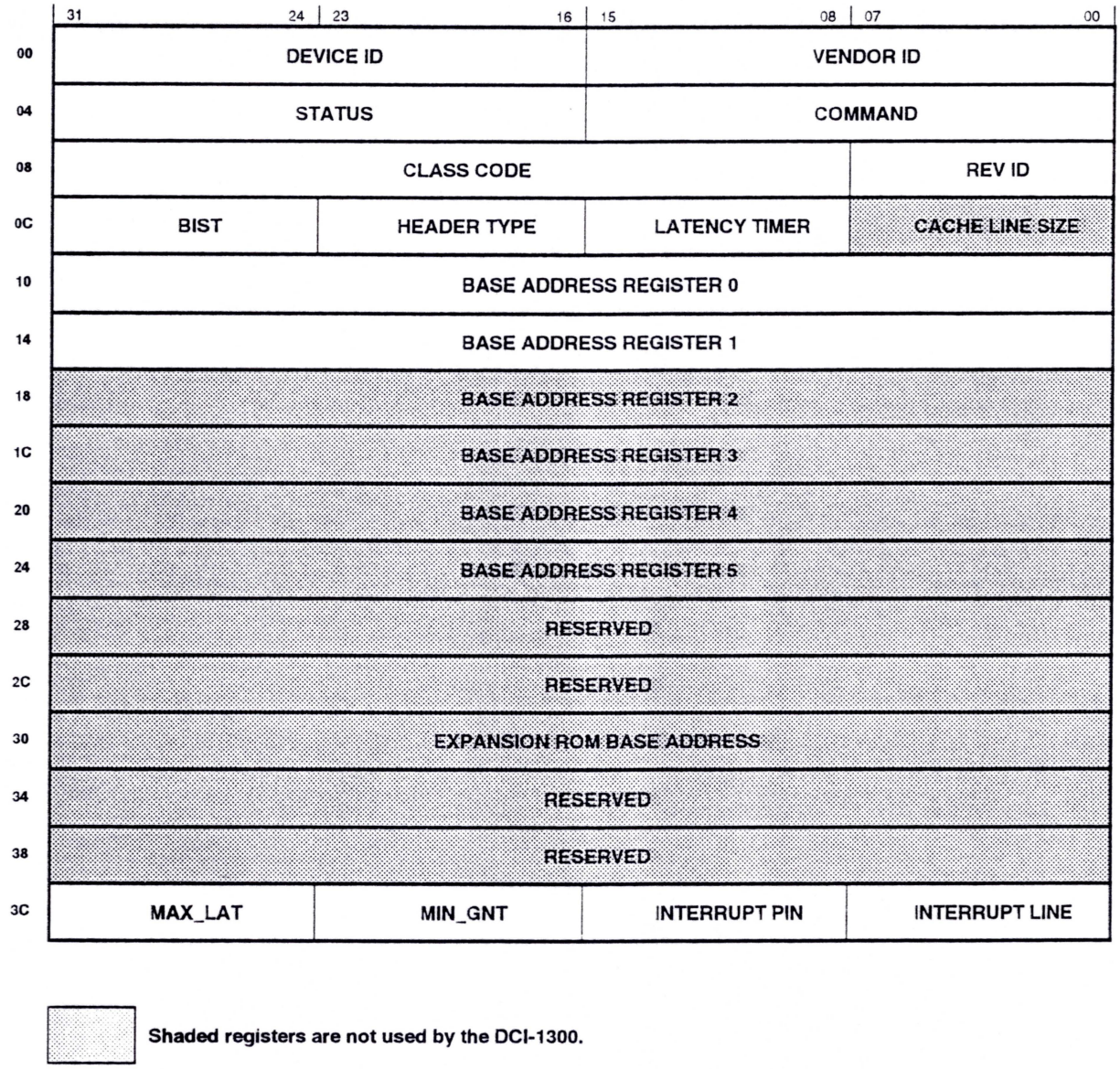


Figure 4-1: PCI Configuration Registers

Identification Register (IDR)

The read-only Identification register contains the vendor and device identification numbers. Write operations from the DCI-1300 have no effect on this register. After reset is removed, this field is boot-loaded from the on-board PROM. The DID and VID numbers are assigned by the PCI Special Interest Group to uniquely identify the manufacture and device.

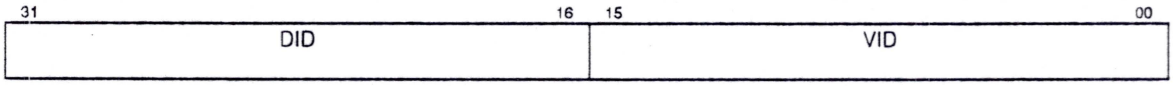


Figure 4-2: Identification Register Bits

Bit	Name	Function
00-15	VID	Vendor ID. This field contains the vendor identification for The Logical Company. Write operations from the PCI interface have no effect on this field. After reset is removed, this field is boot-loaded from the on-board PROM. The value of this field is 10E8 hex.
16-31	DID	Device ID. This field contains the device identification number assigned to the DCI-1300. Write operations from the PCI interface have no effect on this field. After reset is removed, this field is boot-loaded from the on-board PROM. The value of this field is 07 hex.

PCI Status and Command Register (SCR)

The PCI Status and Command register contains PCI command and status information. The lower 16 bits contain read/write command information. The upper 16 bits are a read/write clear field containing the PCI status information. Most status bits within this register are designated as "write clear," meaning that in order to clear a given bit the bit must be written as a one. All bits written with a zero are left unchanged. The value contained in this register after reset is 00800007.

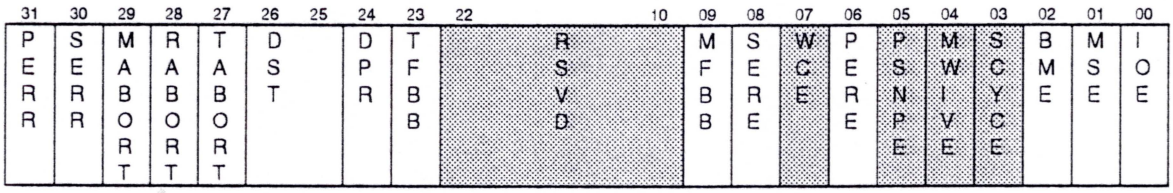


Figure 4-3: PCI Status and Command Register Bits

Bit	Name	Function
00	IOE	I/O Space Enable. This bit allows the DCI-1300 to decode and respond as a target to I/O cycles to regions defined by any one of the five base address registers. This bit is initialized to zero upon assertion of PCI signal RST#.
01	MSE	Memory Space Enable. This bit allows the DCI-1300 to decode and respond as a target for memory regions that may be defined in one of the five base address registers. This bit is initialized to zero upon assertion of PCI signal RST#.
02	BME	Bus Master Enable. When set to a one, this bit allows the DCI-1300 to function as a bus master. The bit is initialized to zero upon the assertion of PCI signal RST #.
03	SCYCE	Special Cycle Enable. Devices that are capable of monitoring special cycles can do so when this bit is set to one. The DCI-1300- does not generate or monitor special cycle, so this bit is hardwired to zero.
04	MWIVE	Memory Write and Invalidate Enable. This bit allows certain bus master devices to use the Memory Write and Invalidate PCI bus command when set to one. When set to zero, masters must use the Memory Write command instead. The DCI-1300 does not support this command when operated as a master and therefore it is hardwired to zero.
05	PSNPE	Palette Snoop Enable. This bit is not supported by the DCI-1300 and is hardwired to zero.

Bit	Name	Function
06	PERE	Parity Error Enable. When this bit is set to one, the DCI-1300 checks for parity errors. When a parity error is detected, PCI bus signal PERR is asserted. This bit is cleared and parity checking is disabled upon the assertion of PCI signal RST#.
07	WCE	Wait Cycle Enable. This bit controls Address/data stepping. Since the DCI-1300 never uses stepping, it is hardwired to zero.
08	SERE	System Error Enable. When this bit is set to one it permits the DCI-1300 to drive the open drain output pin PCI signal SERR. This bit is cleared upon PCI signal RST#. The PCI signal SERR pin driven active normally signifies a parity error on the address/control bus.
09	MFBB	Fast Back-to-Back Enable. When set to one, this bit permits the DCI-1300 to perform "fast" back-to-back bus master cycle after completing a write cycle. This feature can be disabled by writing this bit to zero. This bit is cleared to a zero upon PCI signal RST#.
10-22	RSVD	Reserved. Always zeros.
23	TFBB	Fast Back-to-back Capable. This bit is hardwired to one indicating that the DCI-1300 can accept fast back-to-back cycles as a target.
24	DPR	Data Parity Reported. This bit is set when a PCI data parity error is detected for a transfer when the DCI-1300 is master. The parity Error Enable fit in the Command Register must be set in order for this bit to be set. Once set, this bit is only cleared by writing a one or by the assertion of PCI signal RST#.
25-26	DST	Device Select Timing. These bits are read-only and reflect that state of PCI signal DEVSEL when the DCI-1300 is accessed as a target.
27	TABORT	Signaled Target Abort. This bit is set whenever the DCI-1300 aborts a cycle when addressed as a target. This bit is reset by writing a one to this location.
28	RABORT	Received Target Abort. This bit is set whenever an initiated cycle is terminated by the currently addressed target. This bit is reset by writing a one to this location.
29	MABORT	Received Master Abort. This bit is set whenever a bus master abort occurs. This bit can be reset by writing a one to this location.

Bit	Name	Function
30	SERR	System Error. This bit is set whenever PCI signal SERR is asserted. This bit is reset by writing a one to this location.
31	PERR	Parity Error. This bit is set whenever a PCI parity error is detected. It functions independently from the state of Command Register bit 6. This bit is cleared by writing a one to this location.

Class Code and Revision Identification Register (CRR)

The upper 24 bits contains the DCI-1300 PCI class code. The field is divided into three one-byte fields as shown below.

Base Class	FFh	Not a defined class
Sub-Class	00h	
Programming Information	00h	

The lower eight bits contain the read-only revision identification number of the DCI-1300. This field is initially cleared. Write operations from the PCI interface have no effect on this field. After reset is removed, this field is boot-loaded from the on-board PROM.

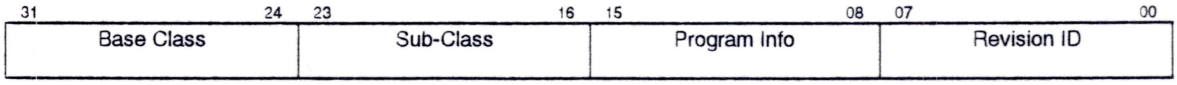


Figure 4-4: Class Code and Revision Identification Register Bits

Bit	Name	Function
00-07	Revision ID	This byte contains the revision number for the DCI-1300. This field is initially cleared. Write operations have no effect on this register. After reset is removed, this field is boot-loaded from the on-board PROM.
08-15	Program Info	This field is boot-loaded with a value of "00h".
16-23	Sub-Class	This byte contains the Sub-class of the DCI-1300 as defined in the PCI specification. The DCI-1300 does not require a sub-class and is boot-loaded from PROM with a value of "00h".
24-31	Base Class	This byte contains the base-class of the DCI-1300 as defined in the PCI specification. The DCI-1300 does not fit in a defined class and is boot-loaded from PROM with a value of "FFh".

Test and Timer Register (TTR)

This register contains self-test, header type, and latency timer information for the DCI-1300. The initial value of the register is boot-loaded from the on-board PROM. Bits 0-7 are hardwaired to zero since the Cache Line Size feature is not supported by the DCI-1300.

The read/write latency timer is used when the DCI-1300 is bus master. Bits 11-15 of the register contain the number of bus clocks remaining for the DCI-1300 to maintain control of the bus. When the DCI-1300 is granted the bus and asserts PCI signal FRAME, the nonzero value for this register is internally decremented. Until the latency timer reaches zero, the DCI-1300 can ignore the removal of bus grant and may continue use of the bus for data transfers.

The Header Type field, bits 16-22, define the format for bytes 10h through 3Fh of the device configuration header.

Read/write bit 23 is set to zero to establish the DCI-1300 as a single function device.

The DCI-1300 does not support built-in self test operations which would utilize bits 24-27 and 30-31.

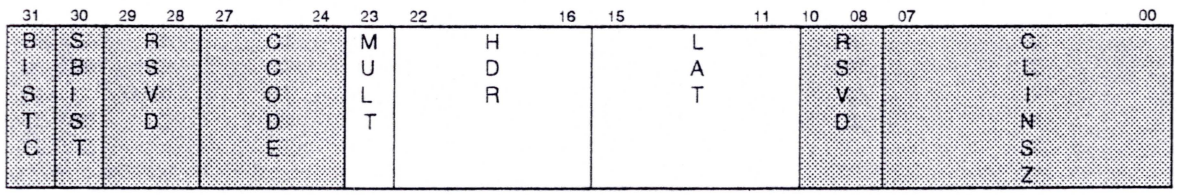


Figure 4-5: Test and Timer Register Bits

Bit	Name	Function
00-07	CLINSZ	Cache Line Size. This field is hardwired to zero since the cache line size feature is not supported by the DCI-1300.
08-10	RSVD	Reserved. These bits are always zero.
11-15	LAT	Latency Timer. This read/write field specifies the number of bus clocks that the DCI-1300 is allowed control of the bus for data transfers as bus master. The value in the field is decremented after the DCI-1300 has been granted the bus and asserted PCI signal FRAME. Prior to the latency count reaching zero, the DCI-1300 can ignore the removal of the bus grant and may continue use of the bus for data transfers.
16-22	HDR	Header Type. This field defines the format for bytes 10h through 3Fh of the device configuration header.

Bit	Name	Function
23	MULT	When set to zero, this bit establishes the DCI-1300 as a single-function device.
24-27	CCODE	Completion Code. Not Used
28-29	RSVD	Reserved. These bits are always zero.
30	SBIST	Start BIST. Self test function not supported by the DCI-1300.
31	BISTC	BIST Capable. This bit always contains a zero to indicate that the DCI-1300 does not support a built-in self test. This bit is read only from the PCI interface.

Base Address Register 0 (BADR0)

Base Address Register 0 provides a mechanism for assigning memory space for the 16 PCI operation registers. The actual memory locations the PCI operation registers respond to are determined by first interrogating Base Address Register 0 to ascertain that the space required is 16 DWORDS, and then writing to Base Address Register 0's high-order field to specify the physical location of the PCI operation registers. This is done by the console firmware. Bit 0 of each field is used to select memory space.

The size of the address space defined by Base Address Register 0 is determined by writing all ones to the register from the PCI bus and then reading the register back. The number of zeros contained in bits 31 through 4 reveals the amount of memory space desired.

After the size of the address space has been determined, the system can allocate memory space for this region and assign it by writing back a value into the bits which contained ones in the Base Address Register 0. This value written back is the physical address assigned to PCI operation registers. For example, Base Address Register 0 returns FFFFFFC0h and is then written with the value 00000300h. This means that the PCI operation registers can be selected for memory addresses between 00000300h through 0000033Fh for this example. The base address value must be on a natural binary boundary for the required size (e.g., 300h, 340h, 380h are valid; 338h is not valid.)

The value of this register is boot-loaded from the on-board PROM after reset with a value of FFFFFFC0h.

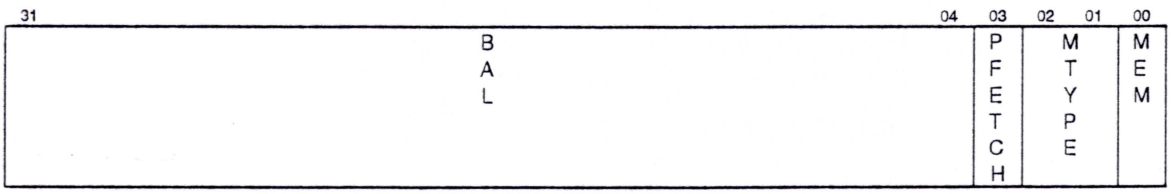


Figure 4-6: Base Address Register 0 Memory Bits

Bit	Name	Function
00	MEM	Memory Space. When set to zero, this bit identifies a base address region as a memory space.

Bit	Name	Function
01-02	MTYPE	Memory type. These two bits identify whether the memory space is 32 or 64 bits wide and if the space location is restricted to be within the first megabyte of memory space. The table below describes the encoding:

Bits 2	Bits 1	Description
0	0	Region is 32 bits wide and can be located anywhere in 32 bit memory space.
0	1	Region is 32 bits wide and must be mapped below the first Mbyte of memory space.
1	0	Not supported.
1	1	Not supported.

03	PFETCH	Prefetchable. Base Address Register 0 always has this bit set to 0. This bit is read only from the PCI interface.
04-31	BAL	Base Address Location. These bits are used to position the decoded region in memory space. Only bits which return a one after being written as one are usable for this purpose.

Base Address Register 1 (BADR1)

Base Address Register 1 provides a mechanism for assigning memory space for the device registers. The actual memory locations the device registers respond to are determined by first interrogating Base Address Register 1 to ascertain the space required is 4 DWORDS, and then writing the Base Address Register 1's high-order field to specify the physical locations of the registers. Bit 0 of each field is used to select memory space.

The size of the address space defined by Base Address Register 1 is determined by writing all ones to the register from the PCI bus and then reading the register back. The number of zeros contained in bits 31 through 4 reveals the amount of memory space desired.

After the size of the address space has been determined, the system can allocate memory space for this region and assign it by writing back a value into the bits which contained ones in the Base Address Register 1. This value written back is the physical address assigned to registers. For example, Base Address Register 1 returns FFFFFFF0h and is then written with the value 00000300h. This means that the registers can be selected for memory addresses between 00000300h through 0000030Fh for this example. The base address value must be on a natural binary boundary for the required size (e.g., 300h, 310h, 320h are valid; 338h is not valid.)

The value in this register is boot-loaded from on-board PROM after reset with a value of FFFFFFF0h.

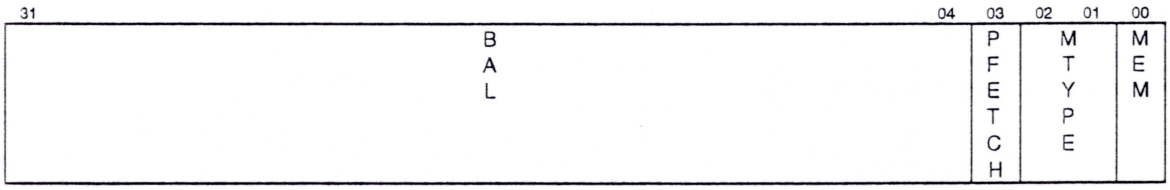


Figure 4-7: Base Address Register 1 Memory Bits

Bit	Name	Function
00	MEM	Memory Space. When set to zero, this bit identifies a base address region as a memory space.

Bit	Name	Function
01-02	MTYPE	Memory type. These two bits identify whether the memory space is 32 or 64 bits wide and if the space location is restricted to be within the first megabyte of memory space. The table below describes the encoding:

Bits 2	Bits 1	Description
0	0	Region is 32 bits wide and can be located anywhere in 32 bit memory space.
0	1	Region is 32 bits wide and must be mapped below the first Mbyte of memory space.
1	0	Not supported.
1	1	Not supported.

03	PFETCH	Prefetchable. Base Address Register 1 always has this bit set to 0. This bit is read only from the PCI interface.
04-31	BAL	Base Address Location. These bits are used to position the decoded region in memory space. Only bits which return a one after being written as one are usable for this purpose. These bits are individually enabled by the contents sourced from the on-board PROM.

Expansion ROM Base Address Register (XROM)

The 32-bit expansion base address ROM register provides a mechanism for assigning a space within physical memory for an expansion ROM. The use of this register is not required to support the functions of the DCI-1300.

Figure 4-8: Expansion ROM Base Address Register Bits

Interrupt/Grant/Latency Register (IGLR)

This register contains interrupt, grant, and maximum latency information. The Maximum Latency field may be optionally used by the DCI-1300 when bus master to specify how often the DCI-1300 needs PCI bus access. The Minimum Grant field may be optionally used by the DCI-1300 when bus master to specify how long of a burst period is needed. The Interrupt Pin field is used to specify which PCI interrupt pin is connected to the DCI-1300 interrupt signal. The Interrupt Line field indicates the interrupt routing for the DCI-1300.

After reset, the value of this register boot-loaded from the on-board PROM to 000001FFh.

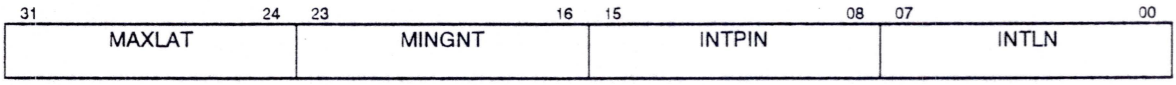


Figure 4-9: Interrupt/Grant/Latency Register Bits

Bit	Name	Function
00-07	INTLN	Interrupt Line. This read/write field indicates the interrupt routing for the DCI-1300. Set to a value of "255" at Reset. May be loaded from on-board PROM after Reset.
08-15	INTPIN	Interrupt Pin. This read-only field identifies which PCI interrupt pin is connected to the DCI-1300 interrupt signal. Value — Interrupt Pin 000 — None 001 — INTA# — Standard 010 — INTB# 011 — INTC# 100 — INTD# Values other than "001" can be loaded from on-board PROM.
16-23	MINGNT	Minimum Grant. Read Only. A value of zero indicates that the bus master has no stringent requirement. Values other than zero can be loaded by the on-board PROM. The units defined by the least significant bit are in 250-ns increments.
24-31	MAXLAT	Maximum Latency. Read Only. A value of zero indicates that the DCI-1300 has no stringent requirements for use of the PCI bus. Values other than zero can be loaded by the on-board PROM. The units defined by the least significant bit are in 250-ns increments.

PCI Operation Registers

The PCI operation registers are mapped as 16 consecutive DWORD registers located at the memory address space specified by the Base Address Register 0. Outgoing Mailbox Register 1 is used to enable PCI interrupts generated by the DCI-1300. The Master Write and Read Address Registers are loaded internally by the DCI-1300 to specify DMA Write and Read addresses, respectively. The Master Write and Read Transfer Count Registers are not used to specify and count the number the number of DMA transfers by the DCI-1300. These functions are performed by other registers within the DCI-1300. MWTC and MRTC registers are required to be loaded with a value of zero to disable their use. The Interrupt Control/Status Register is used to specify the condition to cause a PCI interrupt, a method for viewing the cause of the interrupt, and a method for removing the assertion of the interrupt. The Mailbox Empty-Full Status register is used to view the Outgoing Mailbox empty condition. Figure 4-10 lists the PCI operation registers.

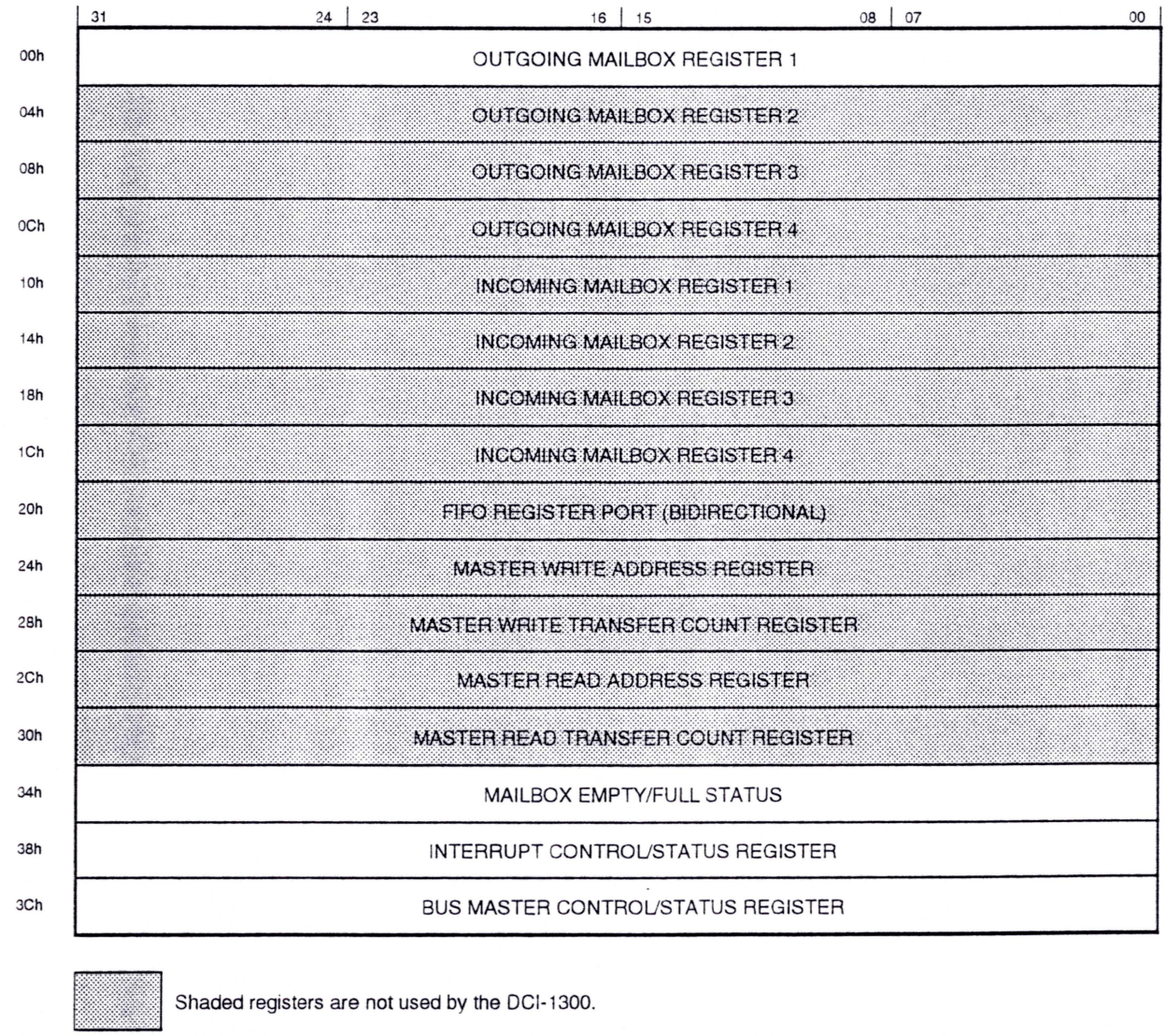


Figure 4-10: PCI Operation Registers

Outgoing Mailbox Register 1 (OMB1) Offset 00h

This read/write DWORD register is used by the DCI-1300 to enable PCI interrupts to be generated by the DCI-1300. The value of this register is unknown following a reset.

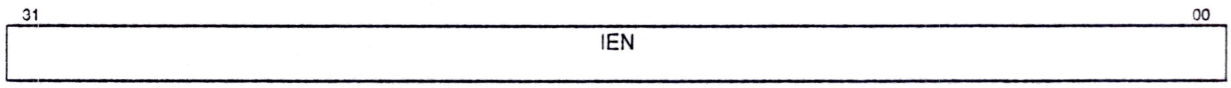


Figure 4-11: Outgoing Mailbox Register 1 Register Bits

Bit	Name	Function
0-31	IEN	Any value written into this register will enable PCI interrupts to be generated by selected DCI-1300 conditions. On detection of a DCI-1300 interrupt condition, internal logic reads this register causing the register to become empty. When selected by software, the empty condition causes an interrupt to be asserted onto the PCI bus. Further DCI-1300 interrupt conditions are blocked from generating a PCI interrupt until the register is written into from the PCI bus and the INTACK register is read. See the device register section for information on the INTACK register.

Master Write Address Register (MWAR) Offset 24h

This register is a 30-bit counter with the low-order two bits hardwired to zero. The register is used to specify the PCI address when moving data to the PCI bus during PCI DMA transfers. This register is not used by the DCI-1300. The value of this register is 00000000h after reset.

Figure 4-12: Master Write Address Register Bits

Bit	Name	Function
00-01	DWORD	Always zero. Read only
02-31	WTAD	Write Transfer Address. Read/Write. When read from the PCI bus, the value of the register specifies the next address to be written into and is incremented following each DWORD data transfer. The register is written from the DCI-1300 with the mapped starting address of the write operation. Writes to this register should not be performed from the PCI bus.

Master Write Transfer Count Register (MWTC) Offset 28h

This register is used to specify the number of bytes to be transferred to the PCI bus during DMA transfers. This function is not used by the DCI-1300. The value of this register is 00000000h after reset.

Figure 4-13: Master Write Transfer Count Register Bits

Bit	Name	Function
00-25	WTCNT	Write Transfer Count. Read/Write. Set to a value of zero during Reset. This register is not used by the DCI-1300/
26-31	RSVD	Reserved. Read/Write. Set to a value of zero during Reset. Should always be a value of zero.

Master Read Address Register (MRAR) Offset 2Ch

This register is a 30-bit counter with the low-order two bits hardwired to zero. The register is used to specify the PCI address when moving data from the PCI bus to the DCI-1300 during PCI DMA transfers. This register is not used by the DCI-1300. The value of this register is 0000000h after reset.

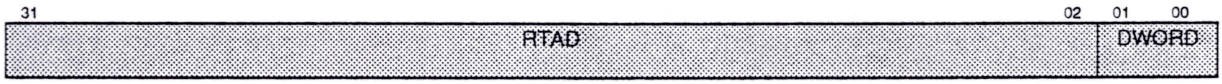


Figure 4-14: Master Read Address Register Bits

Bit	Name	Function
00-01	DWORD	Always zero. Read Only
02-31	RTAD	Read Transfer Address. Read/Write. When read from the PCI bus, the value of the register specifies the next address to be read and is incremented following each DWORD data transfer. This register is not used by the DCI-1300.

Master Read Transfer Count Register (MRTC) — Offset 30h

This register is used to specify the number of bytes to be transferred from the PCI bus during DMA transfers. This function is not used by the DCI-1300. The value of this register is 00000000h after reset.

Figure 4-15: Master Read Transfer Count Register Bits

Bit	Name	Function
00-01	DWORD	Always zero. Read Only
02-31	RTCNT	Read Transfer Count. Read/Write. Set to a value of zero during Reset. This register is not used by the DCI-1300.

Mailbox Empty-Full Status Register (MBEF) Offset 34h

The Mailbox Empty-Full Status register is used to view the Outgoing Mailbox empty condition. The value of this register is 00000000h after reset.

Figure 4-16: Mailbox Empty-Full Status Register Bits

Bit	Name	Function
00-03	EMPTY	Read Only. Set to a value of zero during Reset. Set to a value of all ones when Outgoing mailbox 1 is written into from the PCI bus. A value of zero signifies Outgoing Mailbox 1 has been read and is empty.
04-31	NU	Read only. Set to a value of zero during Reset. The DCI-1300 does not use these bits.

Interrupt Control and Status Register (INTCSR) Offset 38h

The Interrupt Control/Status Register is used to specify the condition to cause a PCI interrupt, a method for viewing the cause of the interrupt, and a method for removing the assertion of the interrupt. Set to value of zero during Reset.

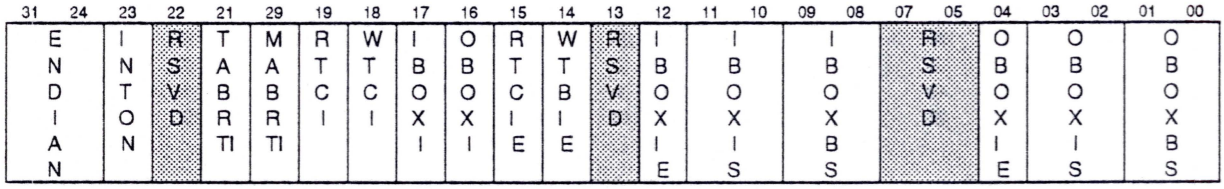


Figure 4-17: Interrupt Control and Status Register Bits

Bit	Name	Function
00-01	OBOXBS	Outgoing Mailbox Byte Select. Read/Write. This field selects which byte of the selected Outgoing Mailboxes is to cause an OBOXI. 00 - byte 0 01 - byte 1 10 - byte 2 11 - byte 3
02-03	OBOXIS	Outgoing Mailbox Interrupt Select. Read/Write. This field selects which of the four Outgoing Mailboxes is to be the source for causing an OBOXI. This field should be set to a value of zero to select Outgoing Mailbox 1 to support DCI-1300 operation.
04	OBOXIE	Outgoing Mailbox Interrupt Enable. Read/Write. When set, this bit enables the generation of anOBOXI.
05-07	RSVD	Reserved. Always zero.
08-09	IBOXBS	Incoming Mailbox Byte Select. Read/Write. This field selects which byte of the selected Incoming Mailboxes is to cause an IBOXI. 00 - byte 0 01 - byte 1 10 - byte 2 11 - byte 3
10-11	IBOXIS	Incoming Mailbox Interrupt Select. Read/Write. This field selects which of the four Incoming Mailboxes is to be the source for causing an IBOXI. This field is not required to support DCI-1300 operation.

Bit	Name	Function
12	IBOXIE	Incoming Mailbox Interrupt Enable. Read/Write. When set, this bit enables the generation of an IBOXI.
13	RSVD	Reserved. Always zero.
14	WTBIE	Write Transfer Complete Interrupt Enable. Read/Write. When set, this bit enables the generation of a WTCI.
15	RTCIE	Read Transfer Complete Interrupt Enable. Read/Write. When set, this bit enables the generation of a RTCI.
16	OBOXI	Outgoing Mailbox Interrupt. When set, this bit indicates an interrupt has been generated due to a read of the Outgoing mailbox selected by bits 04 - 00. The DCI-1300 uses Outgoing Mailbox 1 to support the generation of a PCI interrupt caused by a DCI-1300 condition.
17	IBOXI	Incoming Mailbox Interrupt. When set, this bit indicates an interrupt has been generated due to a write into the Incoming mailbox selected by bits 12 - 08. The DCI-1300 does not use this bit and the bit should always be zero.
18	WTCI	Write Transfer Complete Interrupt. When set, this bit indicates an interrupt has been generated due to the completion of a write transfer and the Write Transfer Count register has reached zero. The DCI-1300 does not use this bit and the bit should always be zero.
19	RTCI	Read Transfer Complete Interrupt. When set, this bit indicates an interrupt has been generated due to the completion of a read transfer and the Read Transfer Count register has reached zero. The DCI-1300 does not use this bit and the bit should always be zero.
20	MABRTI	Master Abort Interrupt. When set, this bit indicates an interrupt has been generated due to the encounter of a Master Abort on the PCI bus. Writing a one to this bit will clear the bit. Writing a zero to this bit leaves the bit unchanged.
21	TABRTI	Target Abort Interrupt. Read/Write-clear. When set, this bit indicates an interrupt has been generated due to a target abort during a DCI-1300 DMA cycle. Writing a one to this bit will clear the bit. Writing a zero to this bit leaves the bit unchanged.
22	RSVD	Reserved. Always zero.
23	INTON	Interrupt Asserted. Read Only. An OR of bits 19-16 and indicates when an interrupt is asserted on the PCI bus.
24-31	ENDIAN	FIFO and Endian Control. Read/Write. Set to a value of zero during Reset.

Bus Master Control and Status Register (MCSR) Offset 3Ch

This read/write register provides for overall control of the DCI-1300. It is used to enable bus mastering for both data directions as well as providing a method to perform software resets. The value of this register is 00000026h after reset.

The following PCI bus controls are available:

- Write Priority over Read
- Read Priority over Write
- Assert reset to internal DCI-1300 logic
- Reset Write (Inbound) FIFO flags
- Reset Read (Outbound) FIFO flags
- Reset mailbox empty full status flags
- Write on-board PROM.

The following PCI interface status flags are provided:

- Read (Outbound) FIFO FULL
- Read (Outbound) FIFO has four or more empty locations
- Read (Outbound) FIFO EMPTY
- Write (Inbound) FIFO FULL
- Write (Inbound) FIFO has four or more words loaded
- Write (Inbound) FIFO EMPTY

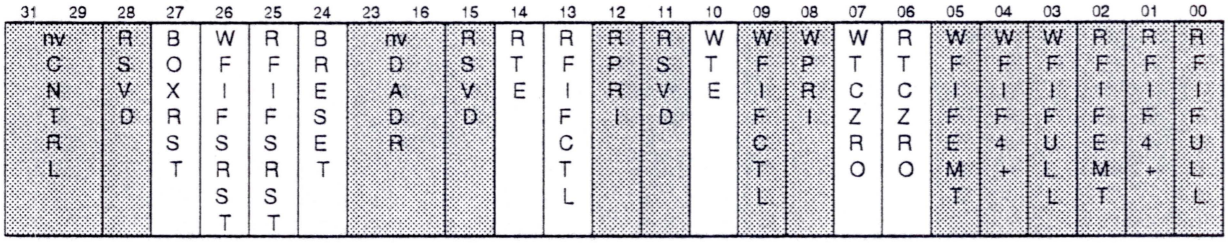


Figure 4-18: Bus Master Control and Status Register Bits

Bit	Name	Function
00	RFIFULL	Read FIFO Full. Read-only. This bit is a one when the outbound PCI bus FIFO is completely full. Not used by the DCI-1300.
01	RFIF4+	Read FIFO 4+ space. Read-only. This bit signifies that there are at least four empty words within the PCI outbound FIFO. Not used by the DCI-1300.

Bit	Name	Function
02	RFIFEMT	Read FIFO Empty. Read-only. This bit is a one when the PCI bus to outbound FIFO is completely empty. Not used by the DCI-1300.
03	WFIFULL	Write FIFO Full. Read-only. This bit is a one when the PCI bus inbound FIFO is completely full. Not used by the DCI-1300.
04	WFIF4+	Write FIFO 4+ Words. Read-only. This bit is a one when there are four or more FIFO words valid within the PCI bus inbound FIFO. Not used by the DCI-1300.
05	WFIFEMT	Write FIFO Empty. Read-only. This bit is a one when the PCI bus inbound FIFO is completely empty. Not used by the DCI-1300.
06	RTCZRO	Read Terminal Count Equals Zero. This read-only bit is set to one to signify that the read transfer count is all zeroes. Not used by the DCI-1300
07	WTCZRO	Write Terminal Count Equal Zero. This read-only bit is set to one to signify that the write transfer count is all zeroes. Not used by the DCI-1300.
08	WPRI	Write versus Read priority. Read/Write. This bit controls the priority of write transfers over read transfers. When this bit is set to a one and bit 12 is zero write transfers always have priority over read transfers. When this bit and bit 12 are both set to ones transfer priorities alternate equally between writes and reads. Not used by the DCI-1300.
09	WFIFCTL	Write FIFO management scheme. Read/Write. When set to a one this bit causes the controller to refrain from requesting the PCI bus unless it has four or more FIFO locations filled. When this bit is zero the controller requests the PCI bus if it has at least one valid FIFO word. Not used by the DCI-1300.
10	WTE	Write Transfer Enable. Read/Write. This bit must be set to a one for PCI bus master write transfers to occur. Writing a zero to this location suspends an active transfer. An active transfer is one in which the terminal count is not zero. This bit is not used by the DCI-1300 and should always be zero.
11	RSVD	Reserved. Always zero.

Bit	Name	Function
12	RPRI	Read versus Write priority. Read/Write. This bit controls the priority of read transfers over write transfers. When set to a one with bit 8 as zero, this indicates that read transfers always have priority over write transfers; when set to a one with bit 8 as one, this indicates that transfer priorities alternate equally between read and writes. Not used by the DCI-1300.
13	RFIFCTL	Read FIFO management scheme. Read/Write. When set to a one, this bit causes the controller to refrain from requesting the PCI bus unless it has four or more vacant FIFO locations to fill. Once the controller is granted the PCI bus or is in possession of the bus due to the write channel this constraint is not meaningful. When this bit is zero the controller requests the PCI bus if it has at least one vacant FIFO word. The DCI-1300 does not use this bit and should always be set to zero
14	RTE	Read Transfer Enable. Read/Write. This bit must be set to a one for PCI bus master read transfer to occur. Writing a zero to this location suspends an active transfer. An active transfer is one in which the terminal count is not zero. This bit is not used by the DCI-1300 and should always be zero.
15	RSVD	Reserved. Always zero.
16-23	nvDADR	Non-volatile memory address/data port. Read/Write. This 8-bit field is used in conjunction with bits 31, 30 and 29 of this register to access the on-board PROM. The contents written are either low address, high address, or data as defined by bits 30 and 29. This register contains the on-board PROM data when the proper read sequence for bits 31 through 29 is performed. Not used by the DCI-1300.
24	BRESET	DCI-1300 reset. Read/Write. Writing a one to this bit causes a reset to the DCI-1300 internal logic to become active. Writing a zero to this pin is necessary to remove the assertion of reset. This bit is read/write.
25	RFIFSRST	Read FIFO Status Reset. Write-only. Writing a one to this bit causes the Outbound (Bus master memory reads) FIFO empty flag to set indicating empty and the FIFO FULL flag to reset and the FIFO Four Plus words available flag to set. It is not necessary to write this bit as zero because it is used internally to produce a reset pulse.

Bit	Name	Function
26	WFIFSRST	Write FIFO Status Reset. Write-only. Writing a one to this bit causes the Inbound (Bus master memory writes) FIFO empty flag to set indicating empty and the FIFO FULL flag to reset and the FIFO Four Plus word flag to reset. It is not necessary to write this bit as zero because it is used internally to produce a reset pulse.
27	BOXRST	Mailbox Flag Reset. Write-Only. Writing a one to this bit causes all mailbox status flags to become reset (EMPTY). It is not necessary to write this bit as zero because it is used internally to produce a reset pulse. Since reading this bit always produces zeroes, this bit is write only.
28	RSVD	Reserved. Always zero.
29-31	nvCNTRL	nvRAM Access Control. Read/Write. This field provides a method for access to the on-board PROM. Write operations are achieved by a sequence of byte operations involving these bits and the 8-bit field of bits 23 through 16. The sequence requires that the low-order address, high order address, and then a data byte are loaded in order. Bit 31 of this field acts as a combined enable and ready for the access to the external memory. D31 must be written to a one before an access can begin, and subsequent accesses must wait for bit D31 to become zero (read). Not used by the DCI-1300.

D31	D30	D29	W/R	
0	X	X	W	Inactive
1	0	0	W	Load low address byte
1	0	1	W	Load high address byte
1	1	0	W	Begin write
1	1	1	W	Begin read
0	X	X	R	Ready
1	X	X	R	Busy

Device Registers

The DCI-1300 has four device registers, while the Digital DRV11 and DR11-C have three. The fourth register contains fields to control data timing and interrupt acknowledges. Reads and writes to the registers must always be 32-bits wide as 8-bit and 16-bit operations are not supported.

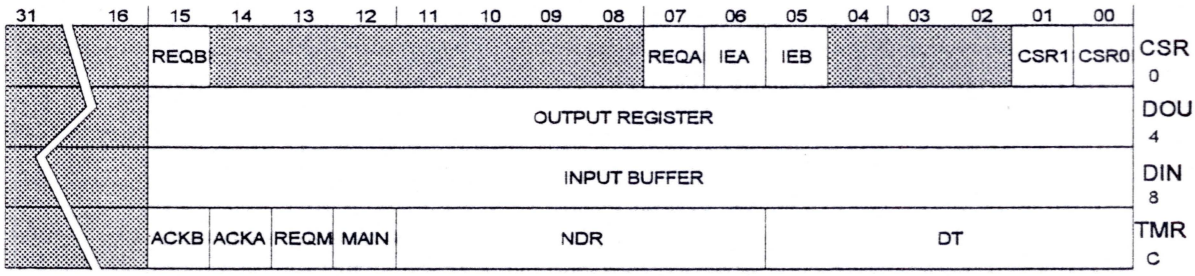


Figure 4-19: DCI-1300 Register Bits

Control/Status Register (CSR)

The CSR is a 32-bit register that controls DCI-1300 functions and monitors status of the DCI-1300 and the interface to the user device. Each of the bits is described in the following.

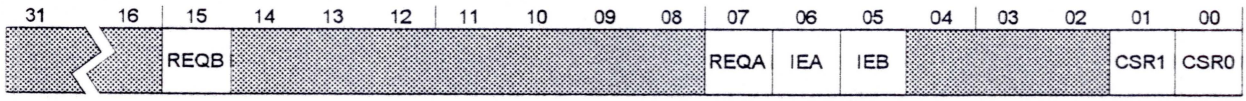


Figure 4-20: Control/Status Register Bits

Bit	Name	Function
31-16		Not used, the value written is ignored and the value read is undefined.
15	REQB	Request B is a read-only bit that reflects the state of the REQB signal from the user's device. It may be used to initiate an interrupt sequence or may be used as a flag that can be tested by software. When used as an interrupt request, assertion by the user device, this bit causes a PCI interrupt request, provided that IEB (bit-5) has been previously set. The interrupt request holds this bit set until acknowledged by writing the ACKB bit in the TMR register. Writing a 0 to this bit is ignored by the controller. When the maintenance loopback cable is attached, this bit is connected to CSR1 (bit-1). This permits diagnostics to write a 0 or 1 into CSR1 and then verify that REQB has the same value.

Bit	Name	Function
14-08		Not used, the value written is ignored and the value read is undefined.
07	REQA	Request A is a read-only bit that reflects the state of the REQA signal from the user's device. It may be used to initiate an interrupt sequence or may be used as a flag that can be tested by software. When used as an interrupt request, assertion by the user device, this bit causes a PCI interrupt request, provided that IEA (bit-6) has been previously set. The interrupt request holds this bit set until acknowledged by writing the ACKA bit in the TMR register. Writing a 0 to this bit is ignored by the controller. When the maintenance loopback cable is attached, this bit is connected to CSR0 (bit-0). This permits diagnostics to write a 0 or 1 into CSR0 and then verify that REQA has the same value.
06	IEA	Interrupt Enable A is a read/write bit that when set allows a PCI interrupt to be generated if REQA (bit-7) has been previously set or when REQA transitions from 0 to 1. Bus reset clears this bit.
05	IEB	Interrupt Enable B is a read/write bit that when set allows a PCI interrupt to be generated if REQB (bit-15) has been previously set or when REQB transitions from 0 to 1. Bus reset clears this bit.
04-02		Not used, the value written is ignored and the value read is undefined.
01	CSR1	CSR1 is a read/write bit that software can use to control the user device. The current value of CSR1 is connected to the user device through interconnect cable J1. When the maintenance loopback cable is attached, this bit is connected to REQB (bit-15). Bus reset clears this bit.
00	CSR0	CSR0 is a read/write bit that software can use to control the user device. The current value of CSR0 is connected to the user device through interconnect cable J2 When the maintenance loopback cable is attached, this bit is connected to REQA (bit-7). Bus reset clears this bit.

Data Output Register (DOUT)

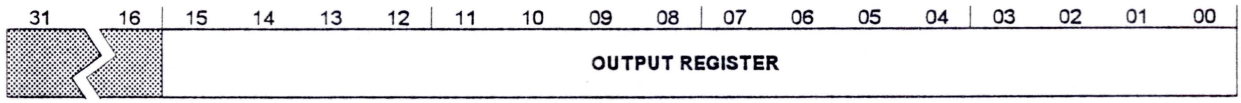


Figure 4-21: Data Output Register Bits

The DOUT is 32-bit read/write register. Writing to this register stores the lower 16-bit of the PCI data bus and presents the data to the user device. When read, the upper 16-bits are undefined. After a PCI bus reset, the output data lines do not reflect the contents of this register until it has been written.

Data Input Buffer (DIN)

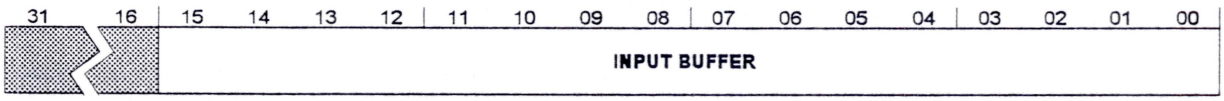


Figure 4-22: Data Input Buffer Bits

The DIN is a 32-bit read-only register. When read, the lower 16-bits contain the current value presented by the user device and the upper 16-bits are undefined.

Timer Register (TMR)

The TMR is a 32-bit read/write register that contains two separate timer control fields, two maintenance bits, and two interrupt acknowledge bits. These timers allow software to adjust the duration of the data transfer strobes sent to the user device. Bus reset clears this register.

Note: The TMR register is unique to the DCI-1300 and does not exist in the Digital DRV11 or DR11-C.

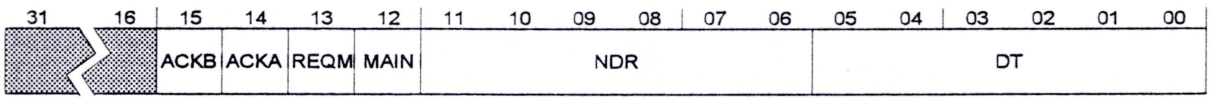


Figure 4-23: Timer Register Bits

Bit	Name	Function
31-16		Not used, the value written is ignored and the value read is undefined.
15	ACKB	Acknowledge B is a special write-only bit that always reads as a 0. Writing a 1 to this bit will remove the REQB generated PCI interrupt request. This operation would be performed by an interrupt service routine to acknowledge and release the REQB PCI interrupt. Writing a 0 to this bit is ignored by the controller.
14	ACKA	Acknowledge A is a special write-only bit that always reads as a 0. Writing a 1 to this bit will remove the REQA generated PCI interrupt request. This operation would be performed by an interrupt service routine to acknowledge and release the REQA PCI interrupt. Writing a 0 to this bit is ignored by the controller.
13	REQM	When set, the Request Maintenance bit forces REQA and REQB to set.
12	MAIN	When set, the state of REQB and REQA is controlled by REQM (bit-13) rather than the signals from the user equipment. This bit is intended for use by diagnostics.
11-06	NDR	The New Data Ready timer field contains a 6-bit value used to control the duration of the New Data Rdy strobe that is generated whenever the DOUT register is written by software. The New Data Rdy signal is set true for a period equal to 2 times the value in the DT timer field +2 overhead clocks, times the PCI clock of 30 ns. The controller does not modify the value in this field. Table 4.1 contains example values for this field.

Bit	Name	Function
05-00	DT	The Data Transmitted timer field contains a 6-bit value used to control the duration of the Data_Trans strobe that is generated whenever the DIN register is read by software. The Data_Trans signal is set true for a period equal to 2 times the value in the DT timer field +2 overhead clocks, times the PCI clock of 30 ns. The controller does not modify the value in this field. Table 4.1 contains example values for this field.

Timer Field	Overhead	NDR or DT Pulse Duration
6	2	(6 * 2 + 2) = 14 14 * 30ns = 420ns
16	2	(16 * 2 + 2) = 34 34 * 30ns = 1020ns (1.02µs)
33	2	(33 * 2 + 2) = 68 68 * 30ns = 2040ns (2.04µs)

Table 4-1: Timer Examples

The DCI-1300 device drivers set a 420ns pulse width for both timers and a utility program is also supplied with the driver to view or change the timer settings.

Appendix A
PCI Local Bus Interface Connector Pin Assignments

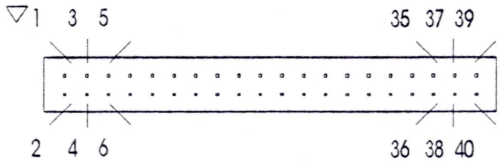
This appendix lists the pin assignments for the PCI bus interface.

Pin	Signal	Pin	Signal
A1	TRST-L	B1	-12V
A2	+12V	B2	TCK-H
A3	TMS-H	B3	GND
A4	TDI-H	B4	TDO-H
A5	+5V	B5	+5V
A6	INTA-L	B6	+5V
A7	INTC-L	B7	INTB-L
A8	+5V	B8	INTD-L
A9		B9	PRSNT1-L
A10	+5V	B10	
A11		B11	PRSNT2-L
A12	GND	B12	GND
A13	GND	B13	GND
A14		B14	
A15	RST-L	B15	GND
A16	+5V	B16	CLK-H
A17	GNT-L	B17	GND
A18	GND	B18	REQ-L
A19		B19	+5V
A20	AD30-H	B20	AD31-H
A21	+3.3V	B21	AD29-H
A22	AD28-H	B22	GND
A23	AD26-H	B23	AD27-H
A24	GND	B24	AD25-H
A25	AD24-H	B25	+3.3V
A26	IDSEL-H	B26	C/BE3-L
A27	+3.3V	B27	AD23-H
A28	AD22-H	B28	GND
A29	AD20-H	B29	AD21-H
A30	GND	B30	AD19-H

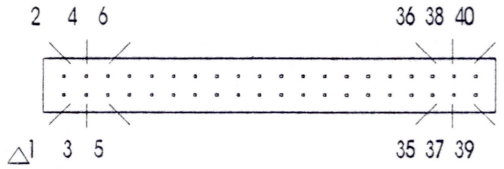
Pin	Signal	Pin	Signal
A31	AD18-H	B31	+3.3V
A32	AD16-H	B32	AD17-H
A33	+3.3V	B33	C/BE2-L
A34	FRAME-L	B34	GND
A35	GND	B35	IRDY-L
A36	TRDY-L	B36	+3.3V
A37	GND	B37	DEVSEL-L
A38	STOP-L	B38	GND
A39	+3.3V	B39	LOCK-L
A40	SDONE-H	B40	PERR-L
A41	SBO-L	B41	+3.3V
A42	GND	B42	SERR-L
A43	PAR-H	B43	+3.3V
A44	AD15-H	B44	C/BE1-L
A45	+3.3V	B45	AD14-H
A46	AD13-H	B46	GND
A47	AD11-H	B47	AD12-H
A48	GND	B48	AD10-H
A49	AD09-H	B49	GND
A50	KEYWAY	B50	KEYWAY
A51	KEYWAY	B51	KEYWAY
A52	C/BE0-L	B52	AD08-H
A53	+3.3V	B53	AD07-H
A54	AD06-H	B54	+3.3V
A55	AD04-H	B55	AD05-H
A56	GND	B56	AD03-H
A57	AD02-H	B57	GND
A58	AD00-H	B58	AD01-H
A59	+5V	B59	+5V
A60	REQ64-L	B60	ACK64-L
A61	+5V	B61	+5V
A62	+5V	B62	+5V

Appendix B
CPX-1303 Panel Connectors

This appendix lists the pin assignments for the DCI-1300 controller and CPX-1303 panel.



40-pin Ribbon Cable Plug



40-pin Ribbon Cable Receptacle

Connector J1

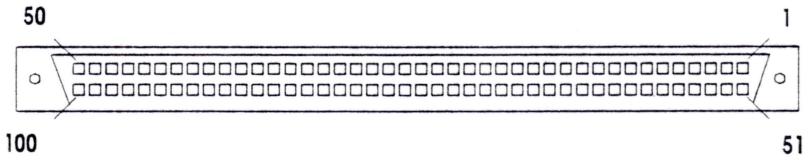
Signal	3M Pin	Berg Pin	Berg Pin	3M Pin	Signal
NEW DATA RDY	1	VV	UU	2	GND
	3	TT	SS	4	GND
OUT02H	5	RR	PP	6	GND
OUT02 H	7	NN	MM	8	GND
REGA H	9	LL	KK	10	GND
OUT15 H	11	JJ	HH	12	OUT14 H
OUT13 H	13	FF	EE	14	GND
CSR1 H	15	DD	CC	16	GND
OUT12 H	17	BB	AA	18	OUT11 H
OUT10 H	19	Z	Y	20	GND
OUT09 H	21	X	W	22	OUT08 H
GND	23	V	U	24	OUT03 H
OUT07 H	25	T	S	26	GND
OUT06 H	27	R	P	28	INIT H
OUT05 H	29	N	M	30	GND
OUT04 H	31	L	K	32	OUT01 H
GND	33	J	H	34	
	35	F	E	36	
	37	D	C	38	OUT00 H
	39	B	A	40	

Connector J2

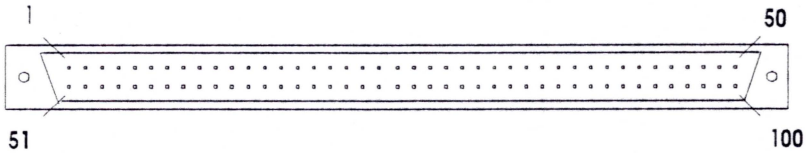
Signal	3M Pin	Berg Pin	Berg Pin	3M Pin	Signal
	1	VV	UU	2	GND
IN00 H	3	TT	SS	4	GND
INITV2 H	5	RR	PP	6	GND
INITV2 H	7	NN	MM	8	GND
IN01 H	9	LL	KK	10	IN04 H
GND	11	JJ	HH	12	IN05 H
	13	FF	EE	14	IN06 H
GND	15	DD	CC	16	IN07 H
IN03 H	17	BB	AA	18	GND
IN08 H	19	Z	Y	20	IN09 H
GND	21	X	W	22	IN10 H
IN11 H	23	V	U	24	IN12 H
GND	25	T	S	26	REQB H
GND	27	R	P	28	IN13 H
IN14 H	29	N	M	30	IN15 H
GND	31	L	K	32	CSR0 H
GND	33	J	H	34	IN02 H
	35	F	E	36	IN02 H
	37	D	C	38	DATA TRANS H
	39	B	A	40	

DCI-1300 Connector Pin Assignments

The high density connector on the DCI-1300 controller (J1) is AMP part number 749076-9 or Thomas & Betts Ansley part number HFR100RA29BX1. It is a 100-pin SCSI style receptacle. Both it and the mating cable connector are shown below. The pin assignments are listed below.



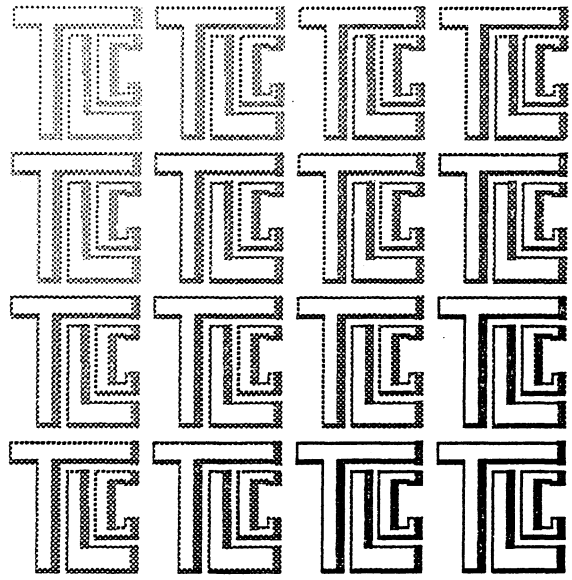
100-pin High Density Panel Receptacle



100-pin High Density Cable Plug

CPX-1303 Connector J3

Pin	Signal	Signal	Pin
1	IN00-H	OUT00-H	51
2	GND	GND	52
3	IN01-H	OUT01-H	53
4	GND	GND	54
5	IN02-H	OUT02-H	55
6	GND	GND	56
7	IN03-H	OUT03-H	57
8	GND	GND	58
9	IN04-H	OUT04-H	59
10	GND	GND	60
11	IN05-H	OUT05-H	61
12	GND	GND	62
13	IN06-H	OUT06-H	63
14	GND	GND	64
15	IN07-H	OUT07-H	65
16	GND	GND	66
17	IN08-H	OUT08-H	67
18	GND	GND	68
19	IN09-H	OUT09-H	69
20	GND	GND	70
21	IN10-H	OUT10-H	71
22	GND	GND	72
23	IN11-H	OUT11-H	73
24	GND	GND	74
25	IN12-H	OUT12-H	75
26	GND	GND	76
27	IN13-H	OUT13-H	77
28	GND	GND	78
29	IN14-H	OUT14-H	79
30	GND	GND	80
31	IN15-H	OUT15-H	81
32	GND	GND	82
33	REQA-H	INITV2-H	83
34	GND	GND	84
35	DATRANS-H		85
36	GND	GND	86
37	REQB-H	+5V	87
38	GND	GND	88
39		+5V	89
40		GND	90
41	INIT-L	+5V	91
42	GND	GND	92
43	CSR0-H	FNCTI3-H	93
44	FNCTI0-H	NEWDARDY-H	94
45	CSR1-H	FNCTI4-H	95
46	FNCTI1-H	FNCTO4-H	96
47	FNCTO2-H	FNCTI5-H	97
48	FNCTI2-H	FNCTO5-H	98
49	GND	P1CLR-L	99
50	P0CLR-L	GND	100



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